1 MHz – 8 GHz, 60 dB Logarithmic Detector/Controller

AD8318

FEATURES

Wide bandwidth: 1 MHz to 8 GHz
High accuracy: ±1.0 dB over 55 dB range (f < 5.8 GHz)
Stability over temperature: ±0.5 dB
Low noise measurement/controller output VOUT
Pulse response time 10/12 ns (fall/rise)
Integrated temperature sensor
Small footprint CSP package
Power-down feature: <1.5 mW at 5 V
Single-supply operation: 5V @ 68 mA
Fabricated using high speed SiGe process

APPLICATIONS

RF transmitter PA setpoint control and level monitoring
RSSI measurement in base stations, WLAN, radar

FUNCTIONAL BLOCK DIAGRAM

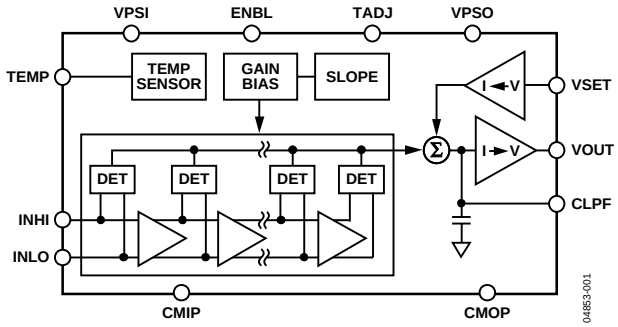

Figure 1.

GENERAL DESCRIPTION

The AD8318 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output voltage. It employs the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell. The device can be used in measurement or controller mode. The AD8318 maintains accurate log conformance for signals of 1 MHz to 6 GHz and provides useful operation to 8 GHz. The input range is typically 60 dB (re: 50 Ω) with error less than ±1 dB. The AD8318 has a 10 ns response time that enables RF burst detection to beyond 60 MHz. The device provides unprecedented logarithmic intercept stability versus ambient temperature conditions. A 2 mV/K slope temperature sensor output is also provided for additional system monitoring. A single supply of +5 V is required. Current consumption is typically 68 mA. Power consumption decreases to <1.5 mW when the device is disabled.

The AD8318 can be configured to provide a control voltage to a VGA, such as a power amplifier or a measurement output, from pin VOUT. Since the output can be used for controller applications, special attention has been paid to minimize wideband noise. In this mode, the setpoint control voltage is applied to VSET. The feedback loop through an RF amplifier is closed via VOUT; the output of which regulates the amplifier's output to a magnitude corresponding to V_{SET}. The AD8318 provides 0 V to 4.9 V output capability at the VOUT pin, suitable for controller applications. As a measurement device, VOUT is externally connected to VSET to produce an output voltage V_{OUT} that is a decreasing linear-in-dB function of the RF input signal amplitude.

The logarithmic slope is nominally −25 mV/dB, but can be adjusted by scaling the feedback voltage from VOUT to the VSET interface. The intercept is +20 dBm (re: 50 Ω, CW input) using the INHI input. These parameters are very stable against supply and temperature variations.

The AD8318 is fabricated on a SiGe bipolar IC process and is available in a 4 mm × 4 mm, 16-pin LFCSP package, for the operating temperature range of −40°C to +85°C.

Rev. 0

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REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS

V_P = 5 V, C_{LPF} = 220 pF, T_A = +25°C, 52.3 Ω termination resistor at INHI, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	INHI (Pin 14) and INLO (Pin 15)				
Specified Frequency Range		0.001		8	GHz
DC Common-Mode Voltage			VPOS – 1.8		V
MEASUREMENT MODE	VOUT (Pin 6) shorted to VSET (Pin 7), sinusoidal input signal				
f = 900 MHz	500 Ω at TADJ to GND				
Input Impedance			957 || 0.71		Ω || pF
±1 dB Dynamic Range	T_A = +25°C		57		dB
	−40°C < T_A < +85°C		48		dB
Maximum Input Level	±1 dB Error		−1		dBm
Minimum Input Level	±1 dB Error		−58		dBm
Slope		−26	−24.5	−23	mV/dB
Intercept		19.5	22	24	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.7	0.78	0.86	V
Output Voltage—Low Power In	P_{IN} = −40 dBm	1.42	1.52	1.62	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		+0.0011		dB/°C
	−40°C ≤ T_A ≤ +25°C		+0.003		dB/°C
f = 1.9 GHz	500 Ω at TADJ to GND				
Input Impedance			523 || 0.68		Ω || pF
±1 dB Dynamic Range	T_A = +25°C		57		dB
	−40°C < T_A < +85°C		50		dB
Maximum Input Level	±1 dB Error		−2		dBm
Minimum Input Level	±1 dB Error		−59		dBm
Slope		−27	−24.4	−22	mV/dB
Intercept		17	20.4	24	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.63	0.73	0.83	V
Output Voltage—Low Power In	P_{IN} = −35 dBm	1.2	1.35	1.5	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		+0.0011		dB/°C
	−40°C ≤ T_A ≤ +25°C		+0.0072		dB/°C
f = 2.2 GHz	500 Ω at TADJ to GND				
Input Impedance			391 || 0.66		Ω || pF
±1 dB Dynamic Range	T_A = +25°C		58		dB
	−40°C < T_A < +85°C		50		dB
Maximum Input Level	±1 dB Error		−2		dBm
Minimum Input Level	±1 dB Error		−60		dBm
Slope		−28	−24.4	−21.5	mV/dB
Intercept		15	19.6	25	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.63	0.73	0.84	V
Output Voltage—Low Power In	P_{IN} = −35 dBm	1.2	1.34	1.5	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		−0.0005		dB/°C
	−40°C ≤ T_A ≤ +25°C		+0.0062		dB/°C

Parameter	Conditions	Min	Typ	Max	Unit
f = 3.6 GHz	51 Ω at TADJ to GND				
Input Impedance			119 || 0.7		Ω || pF
±1 dB Dynamic Range	T_A = +25°C		58		dB
	−40°C < T_A < +85°C		42		dB
Maximum Input Level	±1 dB Error		−2		dBm
Minimum Input Level	±1 dB Error		−60		dBm
Slope			−24.3		mV/dB
Intercept			19.8		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.717		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.46		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		+0.0022		dB/°C
	−40°C ≤ T_A ≤ +25°C		+0.004		dB/°C
f = 5.8 GHz	1000 Ω at TADJ to GND				
Input Impedance			33 || 0.59		Ω || pF
±1 dB Dynamic Range	T_A = +25°C		57		dB
	−40°C < T_A < +85°C		48		dB
Maximum Input Level	±1 dB Error		−1		dBm
Minimum Input Level	±1 dB Error		−58		dBm
Slope			−24.3		mV/dB
Intercept			25		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.86		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.59		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		+0.0033		dB/°C
	−40°C ≤ T_A ≤ +25°C		+0.0069		dB/°C
f = 8.0 GHz	500 Ω at TADJ to GND				
±3 dB Dynamic Range	T_A = +25°C		60		dB
	−40°C < T_A < +85°C		58		dB
Maximum Input Level	±3 dB Error		3		dBm
Minimum Input Level	±3 dB Error		−55		dBm
Slope			−23		mV/dB
Intercept			37		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		1.06		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.78		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		+0.028		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0085		dB/°C
OUTPUT INTERFACE	VOUT (Pin 6)				
Voltage Swing	VSET = 0 V; RFIN = −10 dBm, no load[1]		4.9		V
	VSET = 2.1 V; RFIN = −10 dBm, no load[1]		25		mV
Output Current Drive	VSET = 1.5 V, RFIN = −50 dBm		60		mA
Small Signal Bandwidth	RFIN = −10 dBm; From CLPF to VOUT		600		MHz
Output Noise	RF Input = 2.2 GHz, −10 dBm, f_{NOISE} = 100 kHz, CLPF = 220 pF		90		nV/√Hz

Parameter	Conditions	Min	Typ	Max	Unit
Fall Time	Input Level = off to −10 dBm, 90% to 10%		10		ns
Rise Time	Input Level = −10 dBm to off, 10% to 90%		12		ns
VSET INTERFACE	VSET (Pin 7)				
Nominal Input Range	RFIN = 0 dBm; measurement mode[2]		0.5		
	RFIN = −65 dBm; measurement mode[2]		2.1		V
Logarithmic Scale Factor			−0.04		dB/mV
Bias Current Source	RFIN = −10 dBm; VSET = 2.1 V		2.5		μA
TEMPERATURE REFERENCE	TEMP (Pin 13)				
Output Voltage	T_A = 25°C, R_L = 10 kΩ	0.57	0.6	0.63	V
Temperature Slope	−40°C ≤ T_A ≤ +85°C, R_L = 10 kΩ		2		mV/°C
Current Source/Sink	T_A = 25°C		10/0.1		mA
POWER-DOWN INTERFACE	ENBL (Pin 16)				
Logic Level to Enable Device			1.7		V
ENBL Current When Enabled	ENBL = 5 V		<1		μA
ENBL Current When Disabled	ENBL = 0 V; Sourcing		15		μA
POWER INTERFACE	VPSI (Pins 3, 4), VPSO (Pin 9)				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	ENBL = 5 V	50	68	52	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		68		mA
Supply Current when Disabled	ENBL = 0 V, Total Currents for VPSI and VPSO		260		μA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		350		μA

[1] Controller mode

[2] (Gain = 1) For other gains, see Measurement Mode section of the data sheet.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage: VPSO, VPSI	5.7 V
ENBL, VSET Voltage	0 to VP
Input Power (Single-ended, re: 50 Ω)	12 dBm
Internal Power Dissipation	0.73 W
θ_{JA}[1]	55°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range	260°C

[1]With package die paddle soldered to thermal pads with vias connecting to inner and bottom layers

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

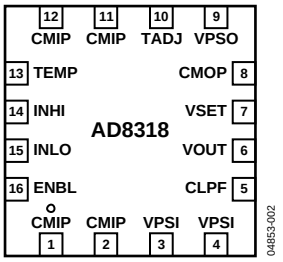

Figure 2. 16-Lead Lead Frame Chip Scale Package (LFCSP)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 11, 12	CMIP	Device Common (Input System Ground).
3, 4, 9	VPSI, VPSO	Positive Supply Voltage for the Device Input System: 4.5 V to 5.5 V (voltage on all pins should be equal).
5	CLPF	Loop Filter Capacitor.
6	VOUT	Measurement and Controller Output.
7	VSET	Setpoint Input for Controller Mode, or Feedback Input for Measurement Mode.
8	CMOP	Device Common (Output System Ground).
10	TADJ	Temperature Compensation Adjustment.
13	TEMP	Temperature Sensor Output.
14	INHI	RF Input. Nominal input range: –60 dBm to 0 dBm re: 50 Ω; ac-coupled RF input.
15	INLO	RF Common for INHI; ac-coupled RF common.
16	ENBL	Device Enable. Connect to VPSI for normal operation. Connect pin to ground for disable mode.
	Paddle	Internally Connected to CMIP, Solder to Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_P = 5 V, T = +25°C, −40°C, +85°C; C_{LPF} = 220 pF; T_{ADJ} = 500 Ω; unless otherwise noted. Colors: +25°C → Black; −40°C → Blue; +85°C → Red

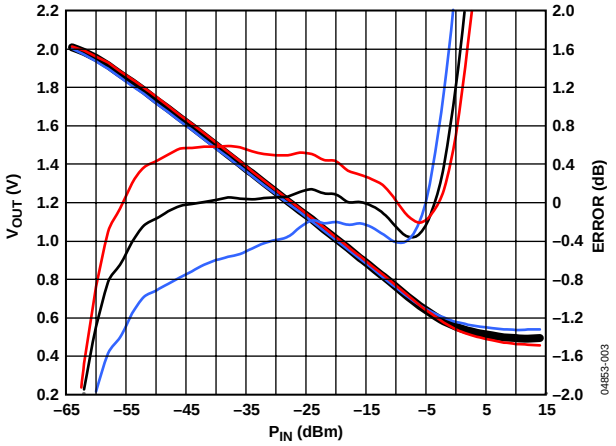

Figure 3. V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz, Typical Device

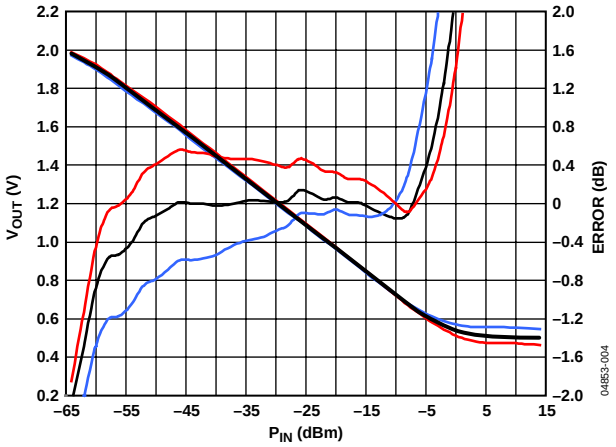

Figure 4. V_{OUT} and Log Conformance vs. Input Amplitude at 1.9 GHz, Typical Device

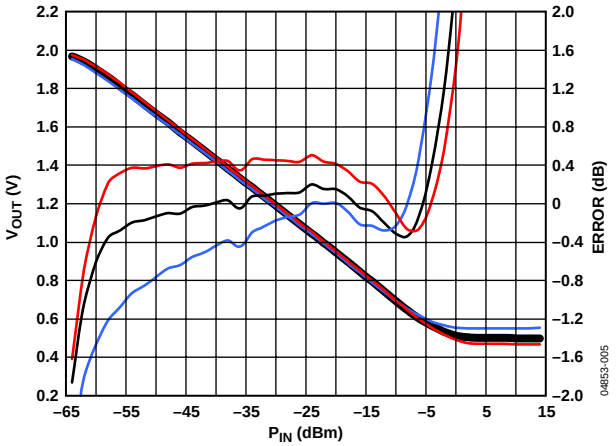

Figure 5. V_{OUT} and Log Conformance vs. Input Amplitude at 3.6 GHz, Typical Device, T_{ADJ} = 51 Ω

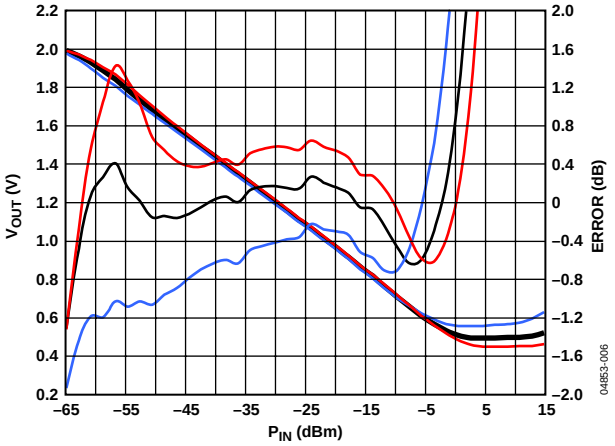

Figure 6. V_{OUT} and Log Conformance vs. Input Amplitude at 5.8 GHz, Typical Device, T_{ADJ} = 1000 Ω

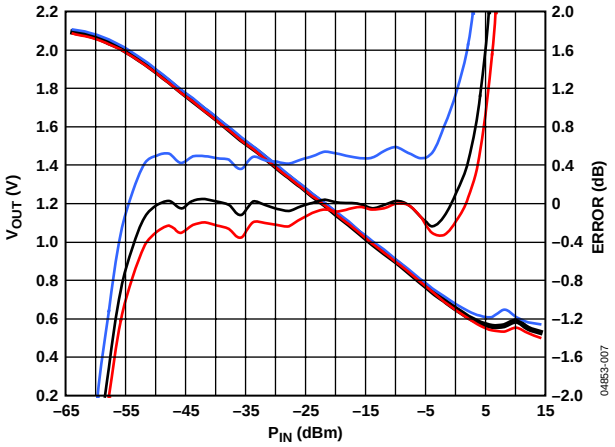

Figure 7. V_{OUT} and Log Conformance vs. Input Amplitude at 2.2 GHz, Typical Device

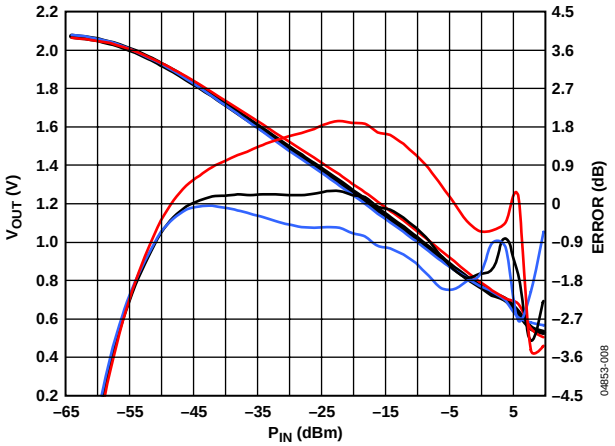

Figure 8. V_{OUT} and Log Conformance vs. Input Amplitude at 8 GHz, Typical Device

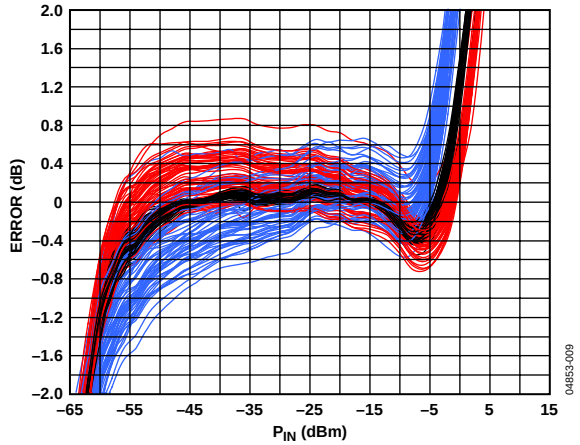

Figure 9. Distribution of Error over Temperature after Ambient Normalization vs. Input Amplitude at 900 MHz for at least 70 Devices

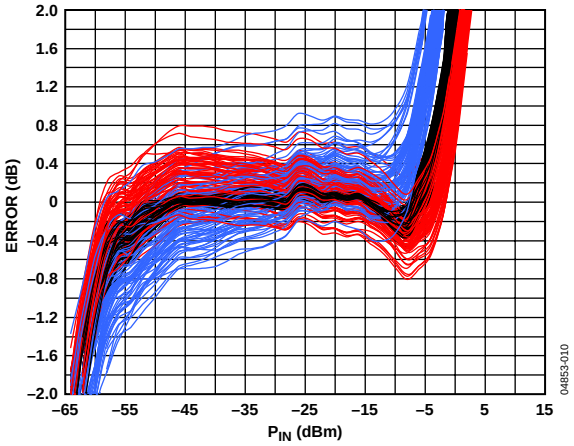

Figure 10. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude at 1900 MHz for at least 70 Devices

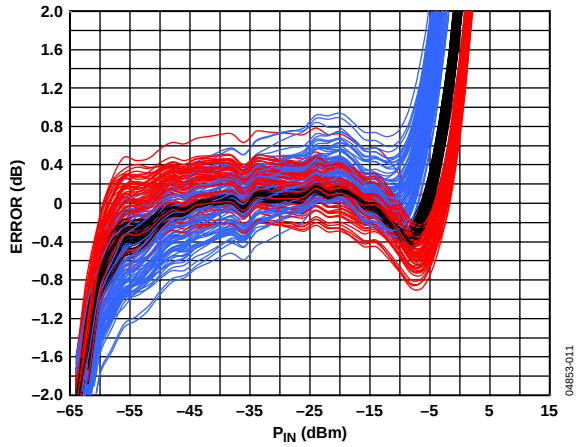

Figure 11. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude at 2.2 GHz for at least 70 Devices

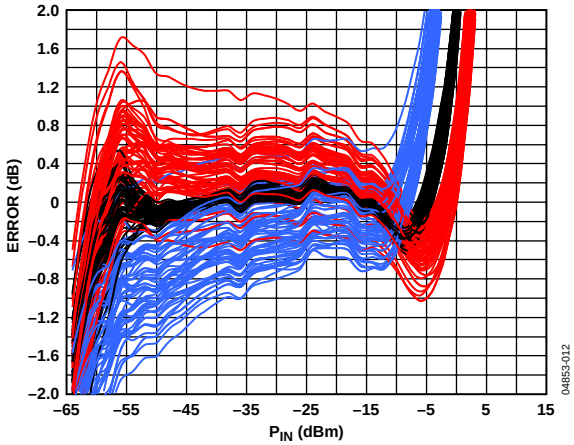

Figure 12. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude at 3.6 GHz for at least 70 Devices

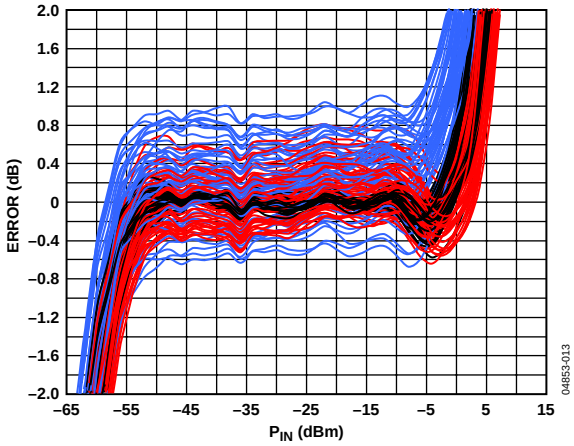

Figure 13. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude at 5.8 GHz (T_{ADJ} =1000 Ω) for at least 70 Devices

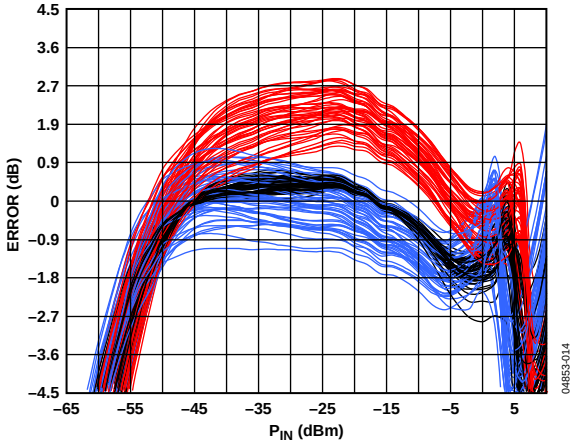

Figure 14. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude at 8 GHz for at least 70 Devices

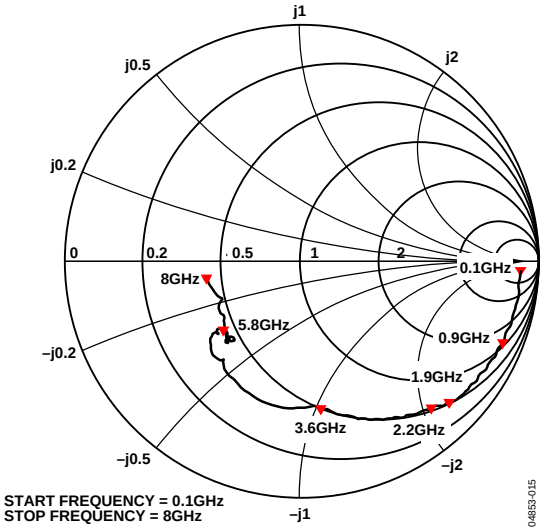

Figure 15. Input Impedance vs. Frequency; No Termination Resistor on INHI

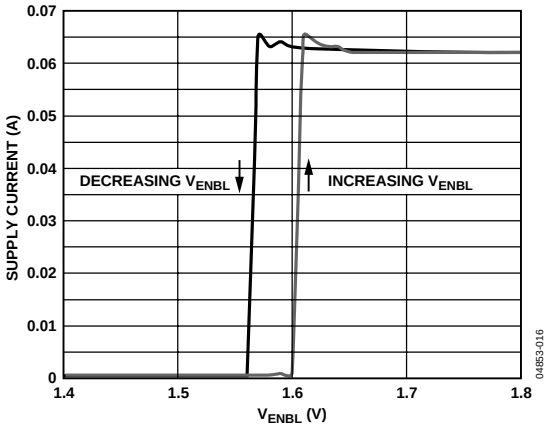

Figure 16. Supply Current vs. Enable Voltage

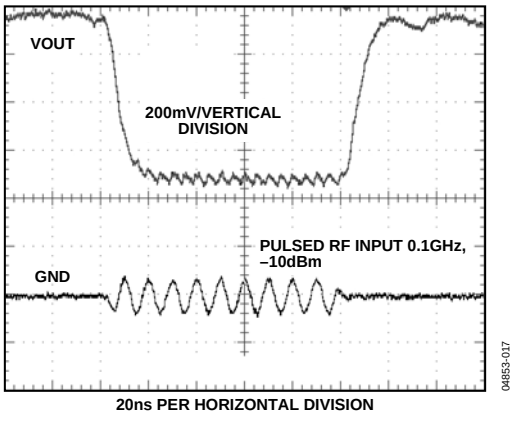

Figure 17. V_{OUT} Pulse Response Time. Pulsed RF Input 0.1 GHz, −10 dBm; C_{LPF} = Open

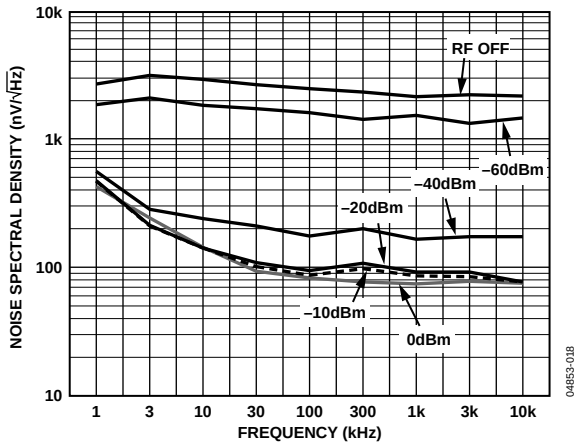

Figure 18. Noise Spectral Density of Output; C_{LPF} = Open

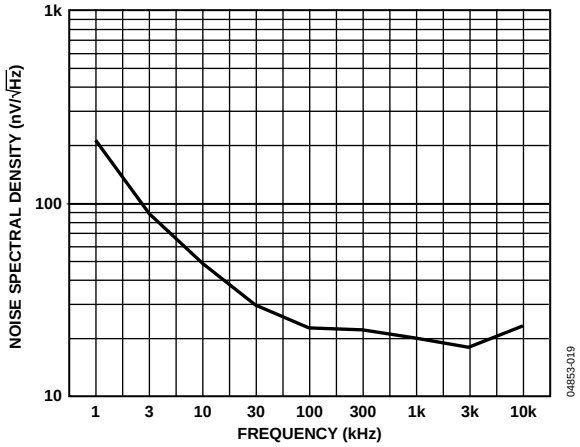

Figure 19. Noise Spectral Density of Output Buffer (from CLPF to VOUT); C_{LPF} = 0.1 µF

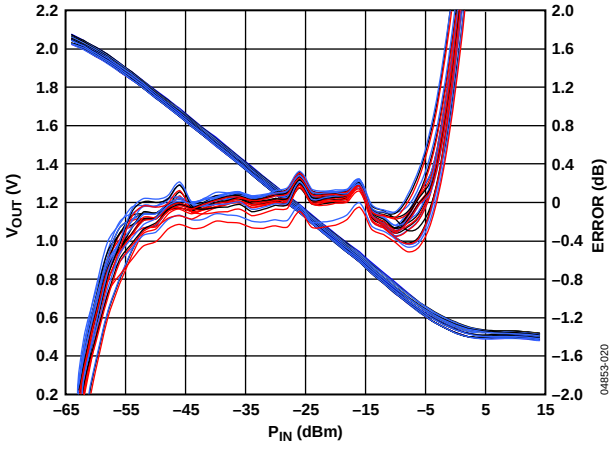

Figure 20. Output Voltage Stability vs. Supply Voltage at 1.9 GHz When V_P Varies by 10%, Multiple Devices

GENERAL DESCRIPTION

The AD8318 is a 9-stage demodulating logarithmic amplifier, which provides RF measurement and power amplifier control functions. The design is similar to the AD8313 Logarithmic Detector/Controller. However, the AD8318 input frequency range is extended to 8 GHz with 60 dB dynamic range. Other improvements include: reduced intercept variability versus temperature, increased dynamic range at higher frequencies, low noise measurement and controller output (VOUT), adjustable low-pass corner frequency (CLPF), temperature sensor output (TEMP), negative transfer function slope for higher accuracy, and 10 ns response time for RF burst detection capability. A block diagram is shown in Figure 21.

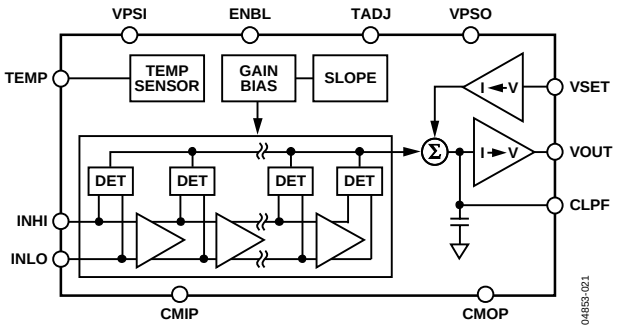

Figure 21. Block Diagram

A fully differential design, using a proprietary high speed SiGe process, extends high frequency performance. Input INHI receives the signal with a low frequency impedance of nominally 1200 Ω in parallel with 0.7 pF. The maximum input with ±1 dB log-conformance error is typically 0 dBm (re: 50 Ω). The noise spectral density referred to the input is 1.15 nV/√Hz, which is equivalent to a voltage of 118 μV rms in a 10.5 GHz bandwidth, or a noise power of –66 dBm (re: 50 Ω). This noise spectral density sets the lower limit of the dynamic range. However, the low-end accuracy of the AD8318 is enhanced by specially shaping the demodulating transfer characteristic to partially compensate for errors due to internal noise. The input system common pin, CMIP, provides a quality low impedance connection to the printed circuit board (PCB) ground through the use of four package pins. The package paddle, which is internally connected to the CMIP pin, should also be grounded to the PCB to reduce thermal impedance from the die to the PCB.

The logarithmic function is approximated in a piecewise fashion by 9 cascaded gain stages. (For a more comprehensive explanation of the logarithm approximation, please refer to the AD8307 data sheet, available at www.analog.com.) The cells have a nominal voltage gain of 8.7 dB each, and a 3 dB bandwidth of 10.5 GHz. Using precision biasing, the gain is stabilized over temperature and supply variations. Since the cascaded gain stages are dc-coupled, the overall dc gain is high. An offset compensation loop is included to correct for offsets within the cascaded cells. At the output of each of the gain stages, a square-law detector cell is used to rectify the signal. The RF signal voltages are converted to a fluctuating differential current having an average value that increases with signal level. Along with the nine gain stages and detector cells, an additional detector is included at the input of the AD8318, altogether providing a 60 dB dynamic range. After the detector currents are summed and filtered, the function $I_D \times \log_{10}(V_{IN}/V_{INTERCEPT})$ is formed at the summing node, where I_D is the internally set detector current, V_{IN} is the input signal voltage, and $V_{INTERCEPT}$ is the intercept voltage (i.e., when $V_{IN} = V_{INTERCEPT}$, the output voltage would be 0 V, if it were capable of going to 0 V).

USING THE AD8318

BASIC CONNECTIONS

The AD8318 is specified for operation up to 8 GHz, as a result low impedance supply pins with adequate isolation between functions are essential. In the AD8318, the two positive supply pins, VPSI and VPSO, must be connected to the same potential. The VPSI pin biases the input circuitry, while the VPSO biases the low noise output driver for VOUT. Separate commons are also included in the device. CMOP is used as the common for the output drivers. All commons should be connected to a low impedance ground plane.

A power supply voltage of between 4.5 V and 5.5 V should be applied to VPS0 and VPS1. 100 pF and 0.1 μF power supply decoupling capacitors should be connected close to each power supply pin. (The two adjacent VPS1 pins can share a pair of decoupling capacitors because of their proximity.)

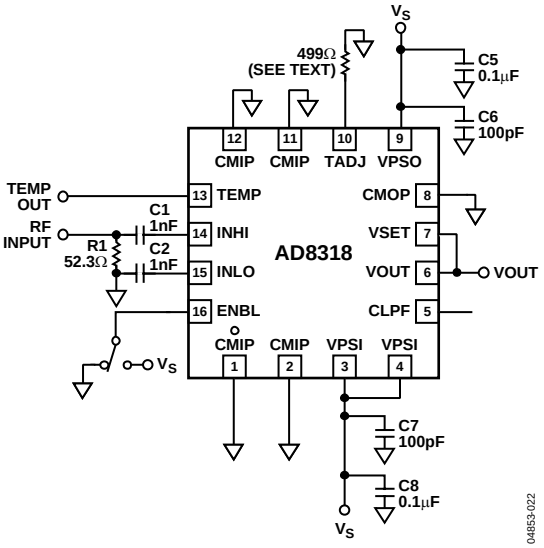

Figure 22. Basic Connections

The paddle of the AD8318's LFCSP package is internally connected to CMIP. For optimum thermal and electrical performance, the paddle should be soldered to a low impedance ground plane.

ENABLE

To enable the AD8318, the ENBL pin must be pulled high. Taking ENBL low will put the AD8318 in sleep mode, reducing current consumption to 260 μA at ambient. The voltage on ENBL must be greater than 2 V_{BE} (~1.7 V) to enable the device. When enabled the devices draws less than 1 μA. When the ENBL pin is pulled low, the pin sources 15 μA.

The enable interface has high input impedance. A 200 Ω resistor is placed in series with the ENBL input for added protection. Figure 23 depicts a simplified schematic of the enable interface.

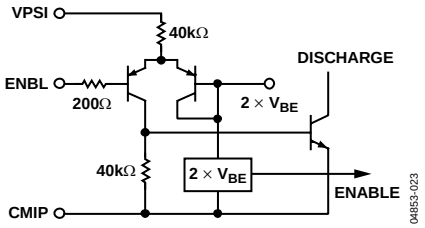

Figure 23. ENBL Interface

INPUT SIGNAL COUPLING

The RF input to the AD8318 (INHI) is single-ended and must be ac-coupled. INLO (input common) should be ac-coupled to ground (See Figure 22). Suggested coupling capacitors are 1 nF ceramic 0402 style capacitors for input frequencies of 1 MHz to 8 GHz. The coupling capacitors should be mounted close to the INHI and INLO pins. These capacitor values can be increased to lower the input stage's high-pass cutoff frequency. The high-pass corner is set by the input coupling capacitors and the internal 10 pF high-pass capacitor. The dc voltage on INHI and INLO will be about one diode voltage drop below V_{PSI}.

The Smith chart in Figure 15 shows the AD8318's input impedance vs. frequency. Table 4 lists the reflection coefficient and impedance at select frequencies. For Figure 15 and Table 4, the 52.3 Ω input termination resistor was removed. At dc, the resistance is typically 2 kΩ. At frequencies up to 1 GHz, the impedance is approximated as 1000 Ω || 0.7 pF. The RF input pins are coupled to a network given by the simplified schematic in Figure 24.

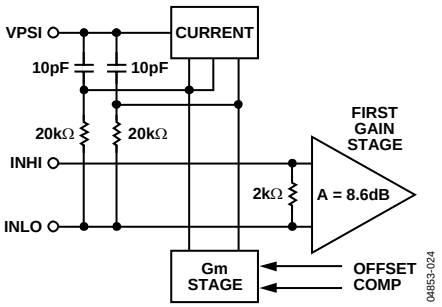

Figure 24. Input Interface

While the input can be reactively matched, in general this is not necessary. An external 52.3 Ω shunt resistor (connected on the signal side of the input coupling capacitors, see Figure 22) combines with the relatively high input impedance to give an adequate broadband 50 Ω match.

Table 4. Input Impedance for Select Frequency

Frequency MHz	S11		Impedance Ω (Series)
	Real	Imaginary	
100	0.918	−0.041	927-j491
456	0.905	−0.183	173-j430
900	0.834	−0.350	61-j233
1900	0.605	−0.595	28-j117
2200	0.524	−0.616	28-j102
3600	0.070	−0.601	26-j49
5300	−0.369	−0.305	20-j16
5800	−0.326	−0.286	22-j16
8000	−0.390	−0.062	22-j3

OUTPUT INTERFACE

The VOUT pin is driven by a PNP output stage. An internal 10 Ω resistor is placed in series with the emitter follower output and the VOUT pin. The rise time of the output is limited mainly by the slew on CLPF. The fall time is an RC limited slew given by the load capacitance and the pull-down resistance at VOUT. There is an internal pull-down resistor of 350 Ω. Any resistive load at VOUT is placed in parallel with the internal pull-down resistor and provides additional discharge current.

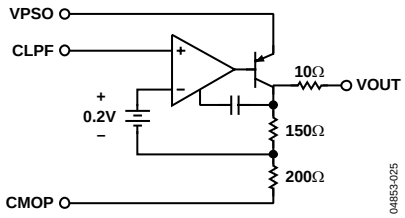

Figure 25. Output Interface

SETPOINT INTERFACE

The V_{SET} input drives the high impedance (250 kΩ) input of an internal op amp. The V_{SET} voltage appears across the internal 3.13 kΩ resistor to generate I_{SET}. When a portion of V_{OUT} is applied to VSET, the feedback loop forces $-I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) = I_{SET}$. If $V_{SET} = V_{OUT}/X$, then $I_{SET} = V_{OUT}/(X \times 3.13\ k\Omega)$. The result is

$$V_{OUT} = (-I_D \times 3.13\ k\Omega \times X) \times \log_{10}(V_{IN}/V_{INTERCEPT})$$

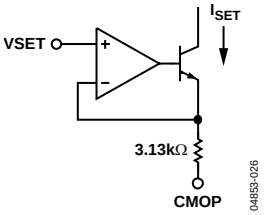

Figure 26. VSET Interface

The slope is given by $-I_D \times X \times 3.13\ k\Omega = -500\ mV \times X$. For example, if a resistor divider to ground is used to generate a V_{SET} voltage of $V_{OUT}/2$, then X = 2. The slope will be set to −1 V/decade or −50 mV/dB.

TEMPERATURE COMPENSATION OF OUTPUT VOLTAGE

The AD8318 functionality includes the capability to externally trim the temperature drift. Attaching a ground-referenced resistor to the T_{ADJ} pin alters an internal current, which works to minimize intercept drift vs. temperature. As a result, the T_{ADJ} resistor can be optimized for operation at different frequencies.

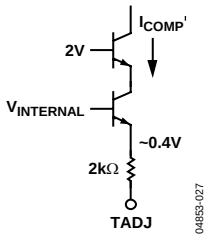

Figure 27. TADJ Interface

A resistor, nominally 500 Ω for optimal temperature compensation at 2.2 GHz input frequency, is connected between this pin and ground (see Figure 22). The value of this resistor partially determines the magnitude of an analog correction coefficient, which is employed to reduce intercept drift.

Table 5 lists recommended resistors for other frequencies. These resistors have been chosen to provide the best overall temperature drift based on measurements of a diverse population of devices.

The relationship between output temperature drift and frequency is not linear and cannot be easily modeled. As a result, experimentation is required to choose the correct T_{ADJ} resistor at frequencies not listed in Table 5.

Table 5. Recommended T_{ADJ} Resistors

Frequency	Recommended T_{ADJ}
900 MHz	500 Ω
1.9 MHz	500 Ω
2.2 GHz	500 Ω
3.6 GHz	51 Ω
5.8 GHz	1 kΩ
8 GHz	500 Ω

TEMPERATURE SENSOR

The AD8318 internally generates a voltage that is proportional-to-absolute-temperature (V_{PTAT}). The V_{PTAT} voltage is multiplied by a factor of 5, resulting in a +2 mV/°C output at the TEMP pin. The output voltage at 27°C is typically 600 mV. An emitter follower drives the TEMP pin, as shown in Figure 28.

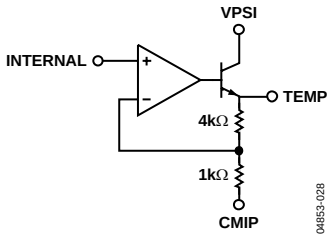

Figure 28. Temp Sensor Interface

The internal pull-down resistance is 5 kΩ. The temperature sensor has a slope of +2 mV/°C.

The temp sensor output will vary with output current due to increased die temperature. Output loads less than 1 kΩ will draw enough current from the output stage causing this increase to occur. An output current of 10 mA will result in the voltage on the temp sensor to increase by 1.5°C, or ~3 mV.

To get the best precision from the temperature sensor, ensure that supply current to AD8318 remains fairly constant (i.e., no heavy load drive).

MEASUREMENT MODE

When the V_{OUT} voltage or a portion of the V_{OUT} voltage is fed back to VSET, the device operates in measurement mode. As seen in Figure 29, the AD8318 has an offset voltage, a negative slope, and a V_{OUT} measurement intercept greater than its input signal range.

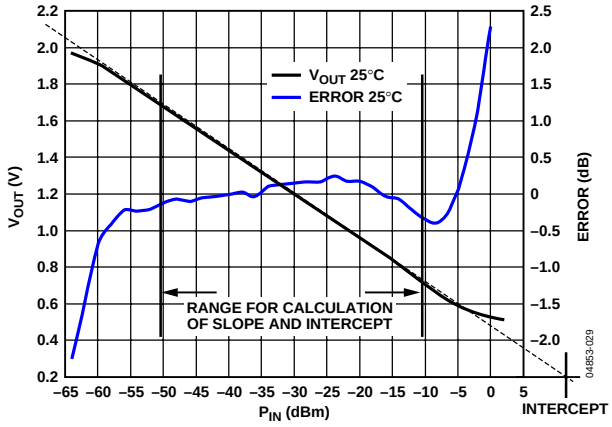

Figure 29. Typical Output Voltage vs. Input Signal

The output voltage versus input signal voltage of the AD8318 is linear-in-dB over a multidecade range. The equation for this function is of the form

$$V_{OUT} = X \times V_{SLOPE/DEC} \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (1)$$

$$= X \times V_{SLOPE/dB} \times 20 \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (2)$$

where:

X is the feedback factor in $V_{SET} = V_{OUT}/X$
$V_{INTERCEPT}$ is expressed in V_{rms}.
$V_{SLOPE/DEC}$ is nominally −500 mV/decade or −25 mV/dB.

$V_{INTERCEPT}$ expressed in dBV is the x-axis intercept of the linear-in-dB transfer function shown in Figure 29. $V_{INTERCEPT}$ is +7 dBV (+20 dBm, re: 50 Ω or 2.239 V_{rms}) for a sinusoidal input signal.

The slope of the transfer function can be increased to accommodate various converter mV per dB (LSB per dB) requirements. However, increasing the slope may reduce the dynamic range. This is due to the limitation of the minimum and maximum output voltages, determined by the chosen scaling factor X.

The minimum value for V_{OUT} is X × V_{OFFSET}. An offset voltage, V_{OFFSET}, of 0.5 V is internally added to the detector signal.

$$V_{OUT(MIN)} = (X \times V_{OFFSET})$$

The maximum output voltage is 2.1 V × X, and cannot exceed 400 mV below the positive supply.

$V_{OUT(MAX)}$ = (2.1 V × X) when X < (V_P – 400 mV)/(2.1 V)

$V_{OUT(MAX)}$ = (V_P – 400 mV) when $X \geq$ (V_P – 400 mV)/(2.1 V)

When X = 1, the typical output voltage swing is 0.5 V to 2.1 V. The output voltage swing can be modeled by using the equations above and restricted by the following equation:

$V_{OUT(MIN)} < V_{OUT} < V_{OUT(MAX)}$

For the case when X = 4 and V_P = 5 V

($X \times V_{OFFSET}$) < V_{OUT} < (V_P – 400 mV)
(4 × 0.5 V) < V_{OUT} < (2.1 V × 4)
2 V < V_{OUT} < 4.6 V

For X = 4, Slope = −100 mV/dB; V_{OUT} can swing 2.6 V, and usable dynamic range will be reduced to 26 dB from 0 dBm to −26 dBm.

The slope is very stable versus process and temperature variation. When base-10 logarithms are used, $V_{SLOPE/DECADE}$ represents the "volts/decade." A decade corresponds to 20 dB, $V_{SLOPE/DECADE}/20 = V_{SLOPE/dB}$ represents the slope in "volts/dB."

As noted in the equations above, the V_{OUT} voltage has a negative slope. This is also the correct slope polarity to control the gain of many power amplifiers and other VGAs in a negative feedback configuration. Since both the slope and intercept vary slightly with frequency, it is recommended to refer to the specification pages for application specific values for slope and intercept.

Although demodulating log amps respond to input signal voltage, not input signal power, it is customary to discuss the amplitude of high frequency signals in terms of power. In this case, the characteristic impedance of the system, Z_o, must be known to convert voltages to their corresponding power levels. Starting with the definitions of dBm and dBV,

$$P(dBm) = 10 \times \log_{10}(V_{rms}^2/(Z_O \times 1\ mW)) \quad (3)$$

$$V(dBV) = 20 \times \log_{10}(V_{rms}/1\ V_{rms}) \quad (4)$$

Expanding Equation 3 gives us:

$$P(dBm) = 20 \times \log_{10}(V_{rms}) - 10 \times \log_{10}(Z_O \times 1\ mW) \quad (5)$$

and given Equation 4, we can rewrite Equation 5 as

$$P(dBm) = V(dBV) - 10 \times \log_{10}(Z_O \times 1\ mW) \quad (6)$$

For example, $P_{INTERCEPT}$ for a sinusoidal input signal expressed in terms of dBm (decibels referred to 1 mW), in a 50 Ω system is:

$$P_{INTERCEPT}(dBm) = V_{INTERCEPT}\ (dBV) - 10 \times \log_{10}(Zo \times 1\ mW) \quad (7)$$

$$= +7\ dBV - 10 \times \log_{10}(50 \times 10^{-3}) = +20\ dBm$$

Further information on the intercept variation dependence upon waveform can be found in the AD8313 and AD8307 data sheets.

AD8318 data sheet specifications for slope and intercept have been calculated based on a best straight line fit using measured data in the −10 dBm to −50 dBm range (see Figure 29).

DEVICE CALIBRATION AND ERROR CALCULATION

The measured transfer function of the AD8318 at 2.2 GHz is shown in Figure 30. The figure shows plots of both output voltage versus input power and calculated error versus input power.

As the input power varies from −65 dBm to 0 dBm, the output voltage varies from 2 V to about 0.5 V.

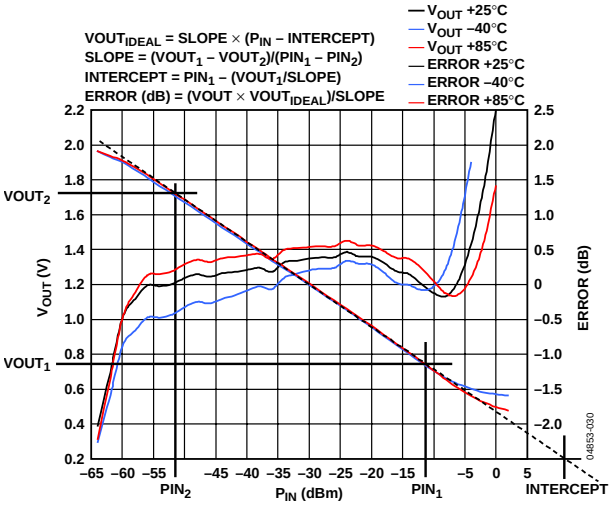

Figure 30. Transfer Function at 2.2 GHz

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy.

We can rewrite the equation for output voltage from the previous section using an intercept expressed in dBm

$$V_{OUT} = Slope \times (P_{IN} - Intercept) \quad (8)$$

In general, the calibration is performed by applying two known signal levels to the AD8318's input and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear-in-dB operating range of the device (see Figure 30). Calculation of slope and intercept is done using the equations

$$Slope = (V_{OUT1} - V_{OUT2})/(P_{IN1} - P_{IN2}) \quad (9)$$

$$Intercept = P_{IN1} - V_{OUT1}/Slope \quad (10)$$

Once *Slope* and *Intercept* have been calculated, an equation can be written which will allow calculation of an (unknown) input power based on the output voltage of the detector.

$$P_{IN}(\text{unknown}) = V_{OUT}(\text{measured})/Slope + Intercept \quad (11)$$

Using the equation for the ideal output voltage (7) as a reference, the log conformance error of the measured data can be calculated:

$$Error(\text{dB}) = (V_{OUT(\text{MEASURED})} - V_{OUT(\text{IDEAL})})/Slope \quad (12)$$

Figure 30 includes a plot of the error at 25°C, the temperature at which the log amp is calibrated. Note that the error is not zero. This is because the log amp does not perfectly follow the ideal V_{OUT} versus P_{IN} equation, even within its operating region. The error at the calibration points (−12 dBm and −52 dBm in this case) will, however, be equal to zero by definition.

Figure 30 also includes error plots for the output voltage at −40°C and +85 °C. These error plots are calculated using the slope and intercept at 25°C. This is consistent with calibration in a mass-production environment where calibration at temperature is not practical.

SELECTING CALIBRATION POINTS TO IMPROVE ACCURACY OVER A REDUCED RANGE

In some applications very high accuracy is required at just one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) will be most critical at or close to full power.

Figure 31 shows the same measured data as Figure 30. Notice that accuracy is very high from −10 dBm to −30 dBm. Below −30 dBm the error increases to about −1 dB. This is because the calibration points have been changed to −14 dBm and −26 dBm.

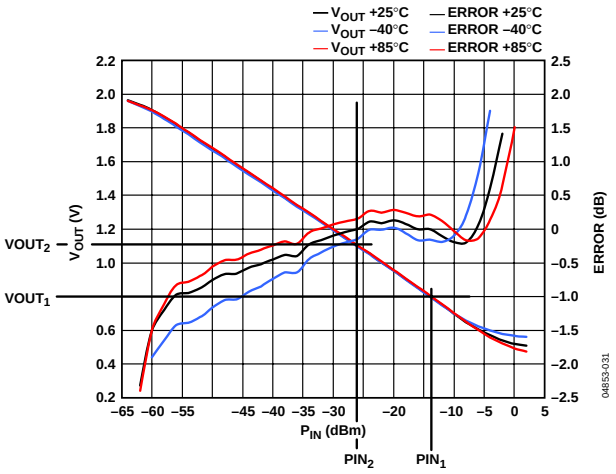

Figure 31. Output Voltage and Error vs. P_{IN} with 2-Point Calibration at −10 dBm and −30 dBm

Calibration points should be chosen to suit the application at hand. In general, though, the calibration points should never be chosen in the nonlinear portion of the log amp's transfer function (above −5 dBm or below −60 dBm in this case).

Figure 32 shows how calibration points can be adjusted to increase dynamic range, but at the expense of linearity. In this case the calibration points for slope and intercept are set at −4 dBm and −60 dBm. These points are at the end of the device's linear range. Once again at 25°C, we see an error of 0 dB at the calibration points. Note also that the range over which the AD8318 maintains an error of < ±1 dB is extended to 60 dB at 25°C and 58 dB over temperature. The disadvantage of this approach is that linearity suffers, especially at the top end of the input range.

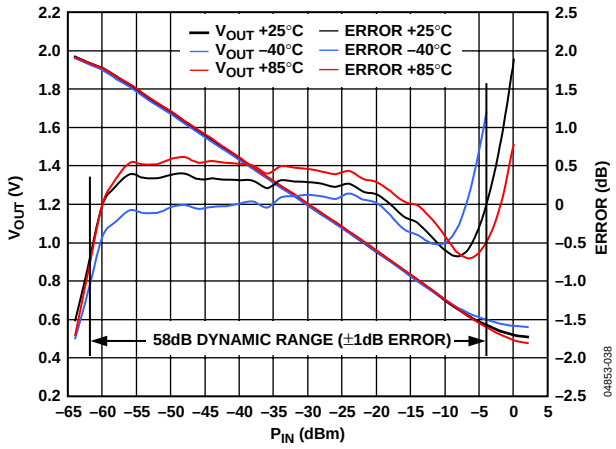

Figure 32. Dynamic Range Extension by Choosing Calibration Points that are Close to the End of the Linear Range

Another way of presenting the error function of a log amp detector is shown in Figure 33. In this case, the dB error at hot and cold temperatures is calculated with respect to the

output voltage at ambient. This is a key difference in comparison to the previous plots. Up to now, all errors have been calculated with respect to the ideal transfer function at ambient.

When we use this alternative technique, the error at ambient becomes by definition equal to 0 (see Figure 33).

This would be valid if the device transfer function perfectly followed the ideal V_{OUT} = Slope × (Pin-Intercept) equation. However since a log amp in practice will never perfectly follow this equation (especially outside of its linear operating range), this plot tends to artificially improve linearity and extend the dynamic range. This plot is a useful tool for estimating temperature drift at a particular power level with respect to the (non-ideal) *output voltage* at ambient. However, to achieve this level of accuracy in an end application would require calibration at multiple points in the device's operating range.

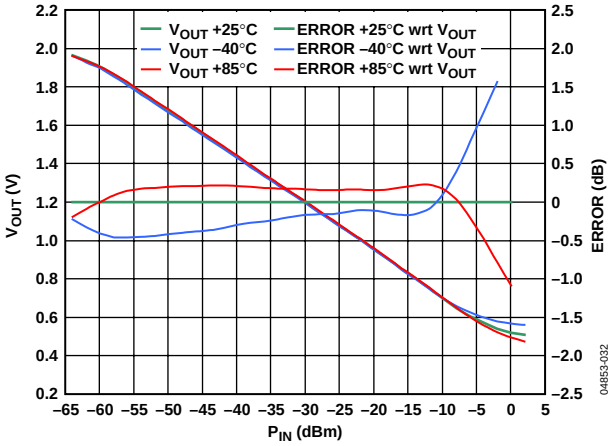

Figure 33. Error vs. Temperature with respect to Output Voltage at 25 °C Does Not Take into Account Transfer Functions' Nonlinearities at 25°C

VARIATION IN TEMPERATURE DRIFT FROM DEVICE TO DEVICE

Figure 34 shows a plot of output voltage and error for multiple AD8318 devices, measured in this case at 5.8 GHz. The concentration of black error plots represents the performance of the population at 25°C (slope and intercept has been calculated for each device). The red and blue plots of error indicate the measured behavior of a population of devices over temperature. This suggests a range on the drift (from device to device) of 1.2 dB.

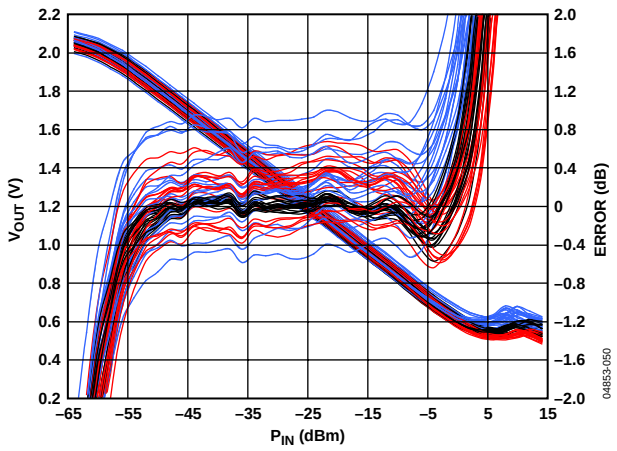

Figure 34. Output Voltage and Error vs. Temperature (+25°C, –40°C, and +85°C) of a Population of Devices Measured at 5.8 GHz

TEMPERATURE DRIFT AT DIFFERENT TEMPERATURES

Figure 35 shows the log slope and error over temperature for a 5.8 GHz input signal. Error due to drift over temperature consistently remains within ±0.5 dB, and only begins to exceed this limit when the ambient temperature drops below −20°C. For all frequencies when using a reduced temperature range higher measurement accuracy is achievable.

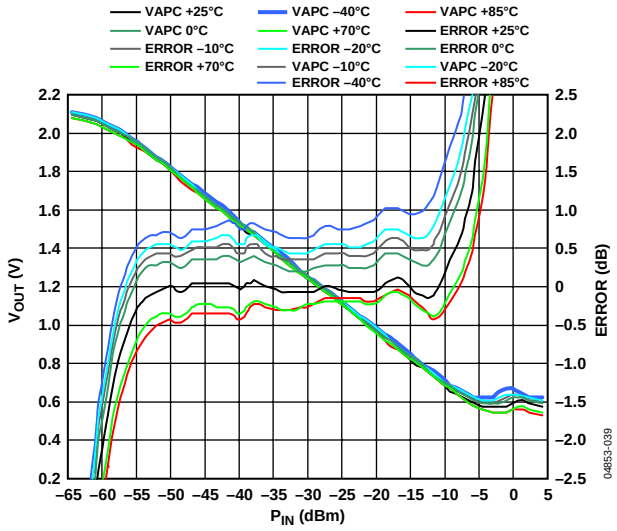

Figure 35. Typical Drift at 5.8 GHz for Various Temperatures

SETTING THE OUTPUT SLOPE IN MEASUREMENT MODE

To operate in measurement mode, VOUT must be connected to VSET. This yields the nominal logarithmic slope of approximately −25 mV/dB. The output swing corresponding to the specified input range will then be approximately 0.5 V to 2.1 V. The slope and output swing

can be increased by placing a resistor divider between VOUT and VSET (i.e., one resistor from VOUT to VSET and one resistor from VSET to common). For example, if two equal resistors are used (e.g., 10 kΩ/10 kΩ), the slope will double to approximately −50 mV/dB. The input impedance of VSET is approximately 500 kΩ. Slope setting resistors should be kept below ~50 kΩ to prevent this input impedance from affecting the resulting slope. When increasing the slope, the new output voltage range cannot exceed the output voltage swing capability of the output stage. Refer to the Measurement Mode section of the data sheet.

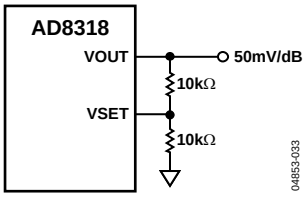

Figure 36. Increasing the Slope

RESPONSE TIME CAPABILITY

The AD8318 has a 10 ns rise/fall time capability (10% – 90%) for input power switching between the noise floor and 0 dBm. This capability enables RF burst measurements at repetition rates to beyond 60 MHz. In most measurement applications, the AD8318 will have an external capacitor connected to CLPF to provide additional filtering for VOUT. However, the use of the CLPF capacitor slows the response time as does stray capacitance on VOUT. For an application requiring maximum RF burst detection capability, the CLPF capacitor pin should be left unconnected. In this case, the integration function is provided by the 700 fF on-chip capacitor.

There is a 10 Ω internal resistor in series with the output driver, an external 40 Ω back-terminating resistor should be added in series at the output when driving a 50 Ω coaxial cable. The back-terminating resistor should be placed close to the VOUT pin. The AD8318 has the drive capability to drive a 50 Ω load at the end of the coaxial cable or transmission line when back terminated. See Figure 37.

The circuit diagram in Figure 37 shows the AD8318 used with a high speed comparator circuit. The 40 Ω series resistor at the output of the AD8318 combines with an internal 10 Ω to properly match to the 50 Ω input of the comparator.

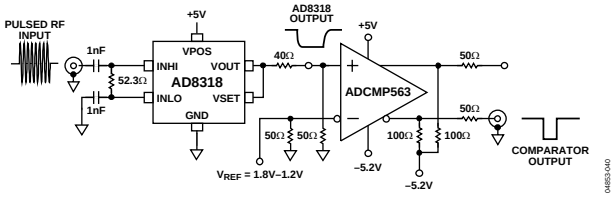

Figure 37. AD8318 Operating with the High Speed ADCMP563 Comparator

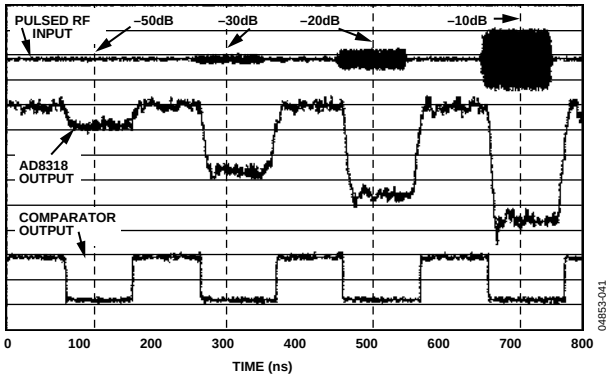

Figure 38. Pulse Response of AD8318 and Comparator for RF Pulses of Varying Amplitudes

Figure 38 shows the response of the AD8318 and the comparator for a 500 MHz pulsed sine wave of varying amplitudes. The output level of the AD8318 is the signal strength of the input signal. For applications where these RF bursts are very small, the output level will not change by a large amount. Using a comparator is beneficial because it will turn the output of the log amp into a limiter-like signal.

CONTROLLER MODE

The AD8318 provides a controller mode feature at the VOUT pin. Using V_{SET} for the setpoint voltage, it is possible for the AD8318 to control subsystems, such as power amplifiers (PAs), variable gain amplifiers (VGAs), or variable voltage attenuators (VVAs) that have output power that increases monotonically with respect to their gain control signal.

To operate in controller mode, the link between VSET and VOUT is broken. A setpoint voltage is applied to the VSET input; VOUT is connected to the gain control terminal of the VGA and the detector's RF input is connected to the output of the VGA (usually using a directional coupler and some additional attenuation). Based on the defined relationship between V_{OUT} and the RF input signal when the device is in measurement mode, the AD8318 will adjust the voltage on VOUT (VOUT is now an error amplifier output) until the level at the RF input corresponds to the applied V_{SET}. When the AD8318 operates in controller mode, there is no defined relationship between V_{SET} and V_{OUT} voltage; V_{OUT} will settle to a value that results in the correct input signal level appearing at INHI/INLO.

In order for this output power control loop to be stable, a ground-referenced capacitor must be connected to the C_{FLT} pin.

This capacitor integrates the error signal (which is actually a current) that is present when the loop is not balanced.

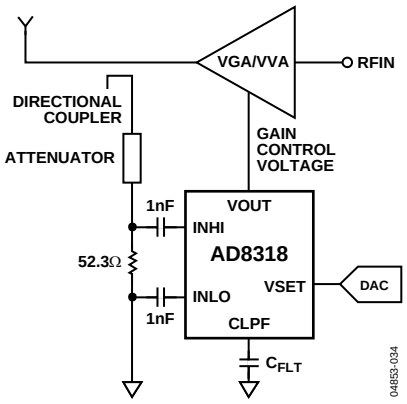

Figure 39. AD8318 Controller Mode

Decreasing V_{SET}, which corresponds to demanding a higher signal from the VGA, will tend to increase V_{OUT}. The gain control voltage of the VGA must have a positive sense that is increasing gain control voltage increases gain.

The basic connections for operating the AD8318 as an analog controller with the AD8367 are shown in Figure 40. The AD8367 is a low frequency to 500 MHz VGA with 45 dB of dynamic range. This configuration is very similar to the one shown in Figure 39.

The gain of the AD8367 is controlled by the voltage applied to the GAIN pin. This voltage, V_{GAIN}, is scaled linear-in-dB with a slope of 20 mV/dB and runs from 50 mV at –2.5 dB of gain, up to 1.0 V at +42.5 dB.

The incoming RF signal to the AD8367 has a varying amplitude level; receiving and demodulating it with the lowest possible error requires that the signal levels be optimized for the highest signal-to-noise ratio (SNR) feeding into the analog-to-digital converters (ADC). This can be accomplished by using an automatic gain control (AGC) loop. In Figure 40 the voltage output of the AD8318 is used to modify the gain of the AD8367 until the incoming RF signal produces an output voltage that is equal to the setpoint voltage V_{SET}.

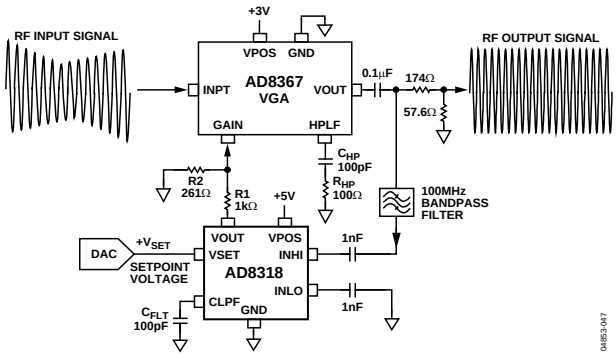

Figure 40. AD8318 Operating in Controller Mode to Provide Automatic Gain Control Functionality in Combination with the AD8367

This AGC loop is capable of controlling signals over ~45 dB dynamic range. The output of the AD8367 is designed to drive loads ≥ 200 Ω. As a result, it is not necessary to use the 53.6 Ω resistor at the input of the AD8318; the nominal input impedance of 2 kΩ is sufficient. If the AD8367's output is to be driving a 50 Ω load, such as an oscilloscope or spectrum analyzer, a simple resistive divider network can be used. Note that the divider used in Figure 40 has an insertion loss of 11.5 dB.

Figure 41 shows the transfer function of output power versus V_{SET} voltage for a 100 MHz sine wave at −40 dBm into the AD8367.

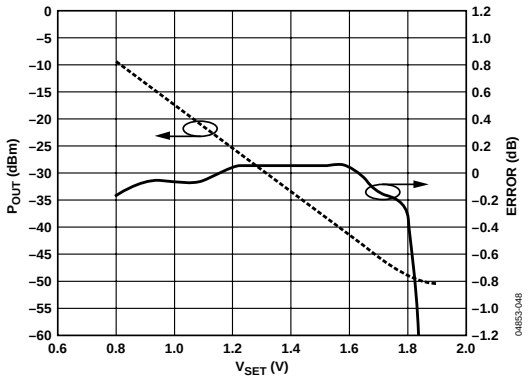

Figure 41. AD8367 Output Power vs. AD8318 Setpoint Voltage

In order for the AGC loop to remain locked, the AD8318 must track the envelope of the VGA's output signal and provide the necessary voltage levels to the AD8367's gain control input. Figure 42 shows an oscilloscope screenshot of the AGC loop depicted in Figure 40. A 50 MHz sine wave with 50% AM modulation is applied to the AD8367. The output signal from the VGA is a constant envelope sine wave with an amplitude corresponding to a setpoint voltage at the AD8318 of 1.0 V.

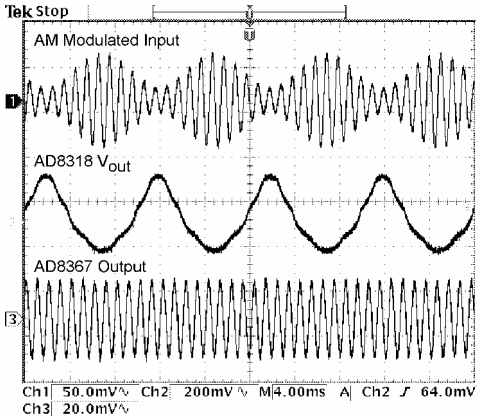

Figure 42. Oscilloscope Screenshot Showing an AM Modulated Input Signal to the AD8367. The AD8318 tracks the envelope of this input signal and applies the appropriate voltage to ensure a constant output from the AD8367.

The 45 dB control range is constant for the range of V_{SET} voltages. The input power levels to the AD8367 must be optimized to achieve this range. In Figure 43 the minimum and maximum input power levels are shown vs. setpoint voltage.

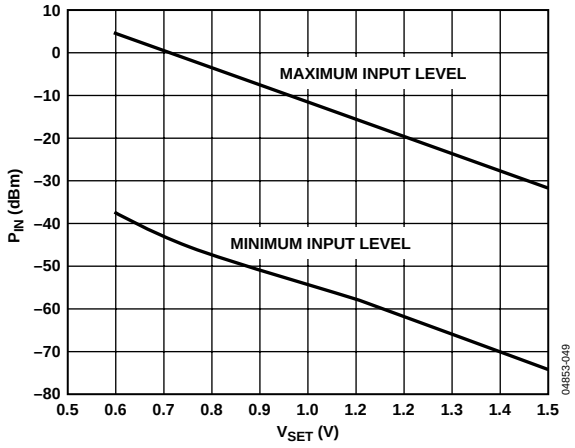

Figure 43. Setpoint Voltage vs. Input Power. Optimal signal levels must be used to achieve the full 45 dB dynamic range capabilities of the AD8367.

In some cases, it may be found that if V_{GAIN} is >1.0 V it may take an unusually long time for the AGC loop to recover; that is, the output of the AD8318 will remain at an abnormally high value and the gain will be set to its maximum level. A voltage divider is placed between the output of the AD8318 and the AD8367's GAIN pin to ensure that V_{GAIN} will not exceed 1.0 V.

In Figure 40, C_{HP} and R_{HP} are configured to reduce oscillation and distortion due to harmonics at higher gain settings. Some additional filtering is recommended between the output of the AD8367 and the input of the AD8318. This will help to decrease the output noise of the AD8367, which may reduce the dynamic range of the loop at higher gain settings (smaller V_{SET}).

Response time and the amount of signal integration are controlled by C_{FLT}—this functionality is analogous to the feedback capacitor around an integrating amplifier. While it is possible to use large capacitors for C_{FLT}, in most applications values under 1 nF will provide sufficient filtering.

Calibration in controller mode is similar to the method used in measurement mode. A simple two-point calibration can be done by applying two known V_{SET} voltages or DAC codes and measuring the output power from the VGA. Slope and intercept can then be calculated with the following equations.

$$Slope = (V_{SET1} - V_{SET2})/(P_{OUT1} - P_{OUT2}) \quad (13)$$

$$Intercept = P_{OUT1} - V_{SET1}/Slope \quad (14)$$

$$V_{SET} = Slope \times (Px - Intercept) \quad (15)$$

More information on AGC applications can be found in the AD8367 Data Sheet.

CHARACTERIZATION SETUPS AND METHODS

The general hardware configuration used for the AD8318 characterization is shown in Figure 45. The primary setup used for characterization was measurement mode. The characterization board is similar to the customer evaluation board with the exception that the RFIN had a Rosenberger SMA connector and R10 was changed to a 1 kΩ resistor to remove cable capacitance from the bench characterization setup. Slope and intercept were calculated using linear regression from −50 dBm to −10 dBm. The slope and intercept are used to generate an ideal line. Log conformance error is the difference from the ideal line and the measured output voltage for a given temperature in dB. For additional information on the error calculation, refer to the Device Calibration and Error Calculation section.

The hardware configuration for pulse response measurement replaced the 0 Ω series resistor on the VOUT pin with a 40 Ω resistor and the CLPF pin was left open. Pulse response time was measured using a Tektronix TDS51504 Digital Phosphor Oscilloscope. Both channels on the scope had 50 Ω termination selected. The 10 Ω internal to the output interface and the 40 Ω series resistor attenuate the output response by 2. RF input frequency was 100 MHz with −10 dBm at the input of the device. The RF burst was generated using SMT06 with the pulse option with a period of 1.5 µS, a width of 0.1 µS, and a pulse delay of 0.04 µS. The output response was triggered using the video out from the SMT06. Refer to Figure 44 for an overview of the test setup.

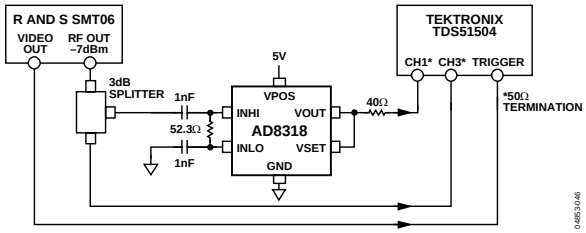

Figure 44. Pulse Response Measurement Test Setup

To measure noise spectral density, the evaluation replaced the 0 Ω resistor in series with the VOUT pin with a 1 µF dc blocking capacitor. The capacitor was used because the FSEA cannot handle dc voltages at the RF input. The CLPF pin was left open for data collected for Figure 18. For Figure 19 a 1 µF capacitor was placed between CLPF and ground. The large capacitor filtered the noise from the detector stages of the log amp. Noise spectral density measurements were made using R&S spectrum analyzer FSEA and R&S SMT06 signal generator. The signal generator's frequency was set to 2.2 GHz. The spectrum analyzer had a span of 10 Hz, resolution bandwidth of 50 Hz, video bandwidth of 50 Hz, and averaged the signal 100 times. Data was adjusted to account for the dc blocking capacitor impedance on the output at lower frequencies.

EVALUATION BOARD

Table 6. Evaluation Board (Rev A) Configuration Options

Component	Function	Default Conditions
TP1, TP2	Supply and Ground Connections	Not Applicable
SW1	Device Enable: When in position A, the ENBL pin is connected to VP and the AD8318 is in operating mode. In position B, the ENBL pin is grounded through R3, putting the device in power-down mode. The ENBL pin may be exercised by a pulse generator connected to J3 with SW1 in position B.	SW1 = A R3 = 10k (Size 0603)
R1, C1, C2	Input Interface: The 52.3 Ω resistor in position R1 combines with the AD8318's internal input impedance to give a broadband input impedance of around 50 Ω. Capacitors C1 and C2 are DC blocking capacitors. A reactive impedance match can be implemented by replacing R1 with an inductor and C1 and C2 with appropriately-valued capacitors .	R1 = 52.3 Ω (Size 0402) C1 = 1 nF (Size 0402) C2 = 1 nF (Size 0402)
R2	Temperature Sensor Interface: The temperature sensor output voltage is available at J1, via the current limiting resistor, R2.	
C4	Temperature Compensation Interface: The internal temperature compensation resistor is optimized for an input signal of 2.2 GHz when C4 is 1 kΩ. This circuit can be adjusted to optimize performance for other input frequencies by changing the value of the resistor in position C4. Note that the designation C4 on the evaluation board is a typographical error as this pad will always be populated with a resistor. This error will be corrected on the Rev B revision of the board.	C4 = 500 kΩ (Size 0603)
R7, R8, R9, R10	Output Interface—Measurement Mode: In measurement mode, a portion of the output voltage is fed back to pin VSET via R7. The magnitude of the slope of the VOUT output voltage response may be increased by reducing the portion of VOUT that is fed back to VSET. R10 can be used as a back-terminating resistor or as part of a single-pole low-pass filter.	R7 = 0 Ω = (Size 0402) R8 = open (Size 0402) R9 = open (Size 0402 R10= 0 Ω (Size 0402)
R7, R8, R9, R10	Output Interface—Controller Mode: In this mode, R7 must be open. In controller mode, the AD8318 can control the gain of an external component. A setpoint voltage is applied to pin VSET, the value of which corresponds to the desired RF input signal level applied to the AD8318 RF input. A sample of the RF output signal from this variable-gain component is selected, typically via a directional coupler, and applied to AD8318 RF input. The voltage at pin VOUT is applied to the gain control of the variable gain element. A control voltage is applied to pin VSET via R9 and R8. The magnitude of the control voltage may optionally be attenuated via the voltage divider comprised of R8 and R9, or a capacitor may be installed in position R8 to form a low-pass filter along with R9.	R7 = open (Size 0402) R8 = open (Size 0402) R9 = 0 Ω (Size 0402) R10 = 0 Ω (Size 0402)
C5, C6, C7, C8, R5, R6	Power Supply Decoupling: The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the AD8318, a 0 Ω series resistor and a 0.1 µF capacitor placed nearer to the power supply input pin.	C6 = 100 pF (Size 0402) C7 = 100 pF (Size 0402) C5 = 0.1 µF (Size 0603) C8 = 0.1 µF (Size 0603) R5 = 0 Ω (Size 0603) R6 = 0 Ω (Size 0603)
C9	Filter Capacitor: The low-pass corner frequency of the circuit that drives pin VOUT can be lowered by placing a capacitor between CLPF and ground.	C4 = open (Size 0603)

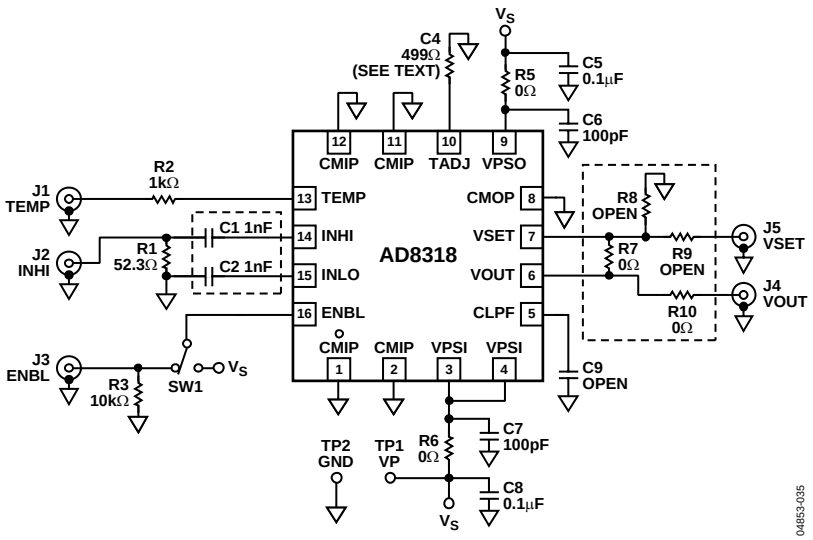

Figure 45. Evaluation Board Schematic (Rev A)

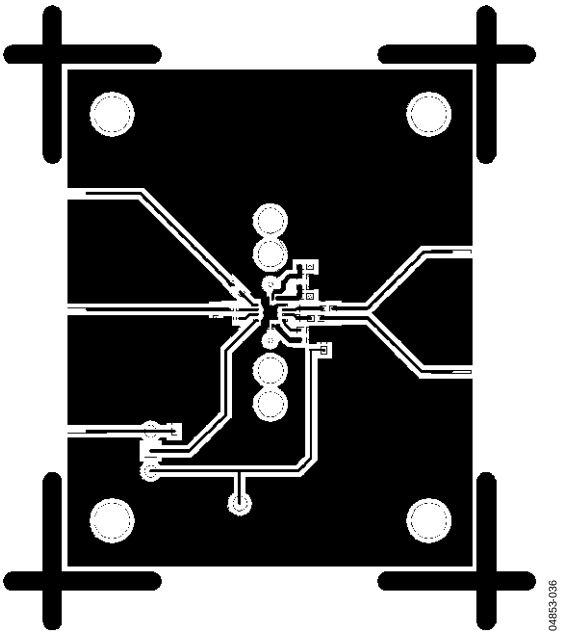

Figure 46. Component Side Layout

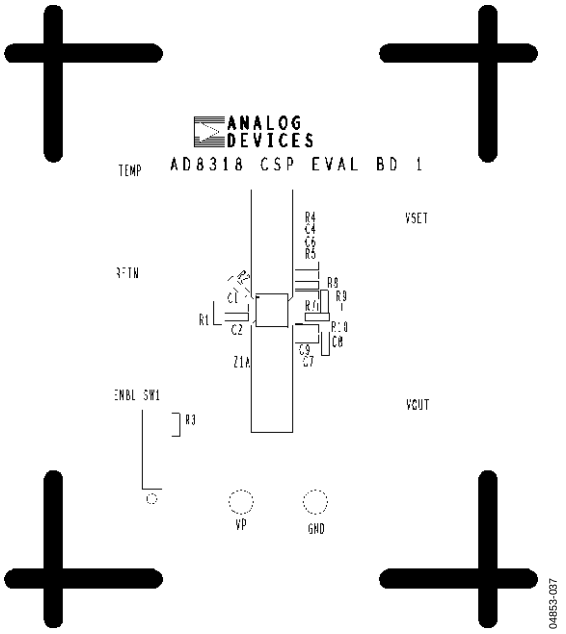

Figure 47. Component Side Silkscreen

OUTLINE DIMENSIONS

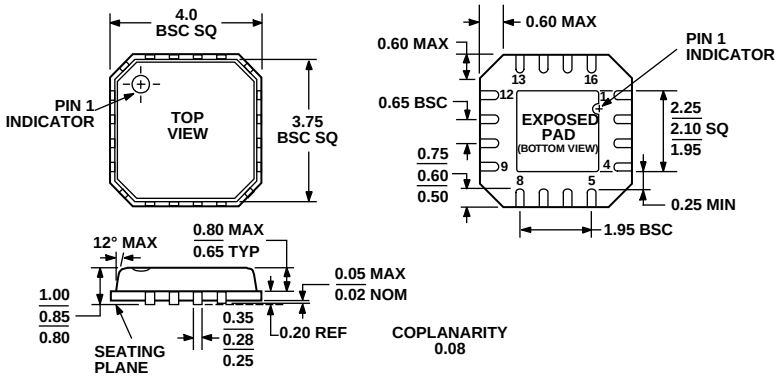

Figure 48. 16-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-16)
Dimensions shown in millimeters

ORDERING GUIDE

AD8318 Products	Temperature Package	Package Description	Package Outline	Ordering Qnty.
AD8318ACPZ-REEL7[1]	–40°C to +85°C	16-Lead LFCSP	CP-16	1500
AD8318ACPZ-WP[1, 2]	–40°C to +85°C	16-Lead LFCSP	CP-16	64
AD8318-EVAL		Evaluation Board		

[1]Z = Pb-free part.

[2]WP = Waffle Pack.

NOTES

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